Customer No.: 31561
Application No.: 10/604,692
Docket No.: 10156-US-PA

REMARKS

Present Status of the Application

Claims 1-12 and 35-45 remain pending. In the outstanding Office Action rejected Claims 1-6, 8, 9 and 35-37 under 35 U.S.C. 102(b) as being anticipated by Yang et al. (US-6,093,945, hereinafter Yang); rejected Claims 1, 7, 10 and 12 under 35 U.S.C. 102(b) as being anticipated by Liang et al. (US-5,714,412, hereinafter Liang); and rejected Claim 11 under 35 U.S.C. 103(a) as being unpatentable over Yang, and further in view of Schwabe et al. (US-4,257,832, hereinafter Schwabe). For at least the following reasons, Applicant respectfully submits that claims 1-12 and 35-45 are in proper condition for allowance. Reconsideration is respectfully requested.

Discussion of the claim rejection under 35 USC 102

1. The Office Action rejected Claims 1-6, 8, 9 and 35-37 under 35 U.S.C. 102(b) as being anticipated by Yang et al. (US-6,093,945, hereinafter Yang).

Applicants respectfully disagree and would like to point out that rejection under 35 U.S.C. 102 requires that each and every elements of the claim(s) must be disclosed exactly by a single prior art reference.

Applicants respectfully submit that Yang cannot anticipate independent Claim 1 because Yang substantially fails to teach or disclose each and every features of the claimed invention as claimed in Claim 1. More specifically, Yang substantially fails to teach or disclose a split-gate non-volatile memory comprising at least [a charge-trapping

layer on the substrate; a split gate on the charge-trapping layer, including at least one split region directly over the charge-trapping layer; wherein the charge-trapping layer around the split region serves as a coding region] as required by the proposed independent claim 1. The advantage of the features recited above is that at least a stronger electric field can be established between the edge portions of the split gate and the p-well that would make it possible to use substantially lower voltages for programming and erasing the split-gate non-volatile memory compared to that used in a conventional memory device.

Instead Yang substantially discloses, in FIGS. 3A-3F, EXAMPLE 1, col. 7, line 41 to col. 8, line 36, a split-gate flash memory cell 100 comprising **[a tunnel oxide layer 13 formed on the substrate 20, and a split gate consisting of a control gate 19 stacked on a pair of matching floating gates 14]** separated by the inter-poly dielectric layer 16. In other words, Yang substantially fails to teach a charge-trapping layer on the substrate; a split gate on the charge-trapping layer, including at least one split region directly over the charge-trapping layer; wherein the charge-trapping layer around the split region serves as a coding region as required by claim 1, instead substantially teaches two opposing floating gates 14 on either sides of the control gate 19 and a tunnel oxide 13 between the control gate 19 and the substrate 20, wherein the two opposing floating gates 14 on either sides of the control gate 19 form the split gate. Accordingly, Applicants respectfully submit that Yang cannot anticipate the proposed independent claim 1 of the claimed invention in this regard.

Furthermore, the layer 13 of Yang, which the Examiner deems as equivalent to

the trapping layer of the claimed invention, is in fact a tunnel oxide layer (please see Fig. 3B, lines 57-58). Applicants respectfully submit that it is well known in the art that in a non-volatile memory, the charge trapping layer is adopted for trapping charges for programming/coding purpose and the tunnel oxide layer is adopted for insulating the gate(s) from the substrate. Therefore, the function of the charge trapping layer and the tunnel oxide layer is completely different, namely the tunneling layer functions to insulate the gate(s) from the substrate and also to allow hot carriers to penetrate there-through during the write and erase operation and not for storing the charges there-in during programming/coding operation. Accordingly, Applicants respectfully submit that the interpretation of the tunnel oxide layer 13 of Yang as equivalent of charge trapping layer is due to an error.

Furthermore, Applicants would like to point out that Yang substantially teaches a conventional flash memory cell including a control gate (19) and two floating gates (14) on either sides of the control gate (19), wherein those skilled in the art would understand that during the programming operation, charges are injected into/or ejected from the floating gates (14) during the programming/erasing operations. In other words, Yang's tunnel oxide layer 13 does not serve as a charge trapping layer as the two floating gates are intended for storing/ejecting the charges during programming/erasing operations. Accordingly, Applicants respectfully submit that the flash memory cell of Yang is not only structurally different but also function quite differently compared to the memory cell of the claimed invention as claimed in claim 1. In other words, as well known in the art, when a flash memory cell comprises floating gates, the charge

trapping layer is not essential as the floating gates are intended for storing/ejecting charges during the programming/erasing operations. Therefore, the tunnel oxide layer 13 of Yang cannot possibly inherently function as a coding region as suggested by the Office Action.

In other words, Yang substantially fails to teach or disclose a split-gate non-volatile memory comprising at least [a charge-trapping layer on the substrate; a split gate on the charge-trapping layer, including at least one split region directly over the charge-trapping layer; and a source/drain in the substrate beside the split gate, wherein the charge-trapping layer around the split region serves as a coding region] as required by the proposed independent claim 1.

Thus, Yang fails to teach, disclose or suggest each and every feature of Claim 1, and therefore Yang cannot possibly anticipate Claim 1 in this regard.

Because the proposed independent claim 35 also recites features that are similar to the proposed independent claim 1, therefore Applicants similarly submit that claim 35 also patently define over Yang for at least the same reasons discussed above.

Claims 2-6, 8 and 9, and claims 36-37 which directly or indirectly depend from independent Claims 1 and 35 respectively are also patentable over Yang at least because of their dependency from an allowable base claim.

For at least the foregoing reasons, Applicant respectfully submits that claims 1-6, 8, 9, and 35-37 are in proper condition for allowance. Reconsideration and withdrawal of above rejections is respectfully requested.

2. The Office Action rejected Claims 1, 7, 10 and 12 under 35 U.S.C. 102(b) as being anticipated by Liang et al. (US-5,714,412, hereinafter Liang).

Applicants respectfully disagree and would like to point out that like Yang, Liang also substantially teach or disclose a conventional flash memory comprising a control gate 20, two floating gates 18', 18'' on either sides of the control gate 20 and a interelectrode dielectric structure (obviously a tunnel oxide layer) 19 between the control gate 20 and the floating gates 18', 18'', and therefore, Applicants similarly submit that Liang cannot possibly anticipate the proposed independent claim 1 for at least the same reasons discussed above.

Claims 7, 10 and 12 which directly or indirectly depend from independent Claim 1 are also patentable over Liang at least because of their dependency from an allowable base claim.

For at least the foregoing reasons, Applicant respectfully submits that claims 1, 7, 10 and 12 are in proper condition for allowance. Reconsideration and withdrawal of above rejections is respectfully requested.

Discussion of the claim rejection under 35 USC 103

The Office Action rejected Claim 11 under 35 U.S.C. 103(a) as being unpatentable over Yang as applied to claim 1 above, and further in view of Schwabe et al. (US-4,257,832, hereinafter Schwabe).

Applicants respectfully disagree and would like to point out that because both Yang and Schwabe (at col. 3, lines 14-15) substantially teach tunnel oxide layer (13, 13) and they both fail to teach, suggest or hint a charge trapping layer, therefore, Yang and schwabe cannot possibly render claim 11 obvious in a manner suggested by the Office Action. For at least the foregoing reasons, claim 11 also patently defines over Yang and Schwabe and should be allowed. Reconsideration and withdrawal of the above rejections is respectfully requested.

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CONCLUSION

For at least the foregoing reasons, it is believed that all pending claims 1-12 and 35-45 are in proper condition for allowance. If the Examiner believes that a conference would be of value in expediting the prosecution of this application, he is cordially invited to telephone the undersigned counsel to arrange for such a conference.

Respectfully submitted,

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